Philips Semiconductors
Content Protection A/V Link Layer
IEEE 1394 Reference Design Kit
Version 2.2 for L4X / P21

Hardware Reference Manual

Philips Semiconductors

Full Duplex A/V Link Layer

1394 L4X Reference Design Kit version 2.2

Hardware Reference Manual

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1 About This Manual

This manual is the technical guide to the hardware design and implementation of the Philips Full Duplex AV Link Layer Evaluation Board. It contains a description of all major functional areas on the board, with explanations where required. It also appends a Bill of Materials for the board, and the complete schematics. Please note that the AV Link chip present on this board may be one of type part numbers: 1) the PDI1394L40 Full Duplex AV Link, or 2) the PDI1394L41 Content Protection AV Link chip, depending upon which kit was purchased.

1.1 Requirements

Before reading this manual and undertaking a 1394 design, it is recommended that you have an understanding of the IEEE 1394 bus specifications. You should also be familiar with the operation and pin-out of the Link and Physical Layer ICs used in this design. The pin-outs of the ICs are available in the data sheets for these parts, in Adobe PDF format.

2 Overview

The Philips Full Duplex Evaluation Board, the physical component of the Philips Full Duplex A/V Link Layer 1394 Reference Design Kit version 2.2, allows you to test and experiment with an example 1394 design. This includes testing and evaluating the provided example software, as well as implementing and testing user modified software that is aimed at a specific application.

A complete list of features of the Evaluation Board follows the functional description and block diagram.

2.1 Functional Description

The Evaluation Board consists of four main functional blocks. A Physical Layer IC, connected to three 1394 ports, handles all physical layer transactions. The Physical Layer IC connects to an AV Link Layer IC, which handles all link layer transactions, and provides a means for packetizing and transmitting/receiving AV data. An AV section, connected to the Link Layer IC, contains a dual AV Data Simulator CPLD, for the generation of test AV data, and two AV headers, to facilitate the connections of external sources and sinks of AV data (for example, a digital set top box, camera, VCR, etc.). Finally, an 8051 flash programmed microcontroller, which handles, through software, all higher network layers, connects to the Link Layer IC.

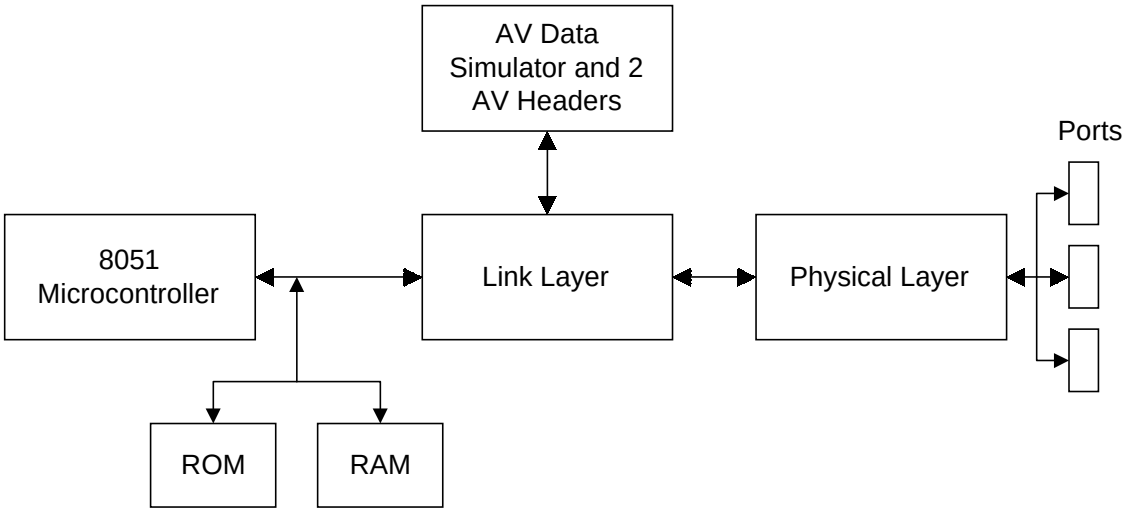


Figure 2-1: Block diagram of Philips 1394 AV Evaluation Board

2.2 Evaluation Board Features

The 1394 AV Evaluation board has the following features:

- RS 232 serial interface to the host PC that allows downloading of 89C51 code to the flash programmable MCU on the board.
- 64K of program space (Flash ROM within the MCU or external socketed EPROM) and 64K of RAM space for data.
- Code is compiled in exactly the same manner, whether it is executed from an EPROM, or the flash ROM in the 89C51 MCU.
- A high speed serial link (RS 232), operating at rates up to 9600 Kbps, between the 89C51 and the host PC.
- An LED (D4) to show active cable connections to the Physical Layer IC.
- A User LED (D2) , which may be turned on or off any time you wish, to aid in software debugging/testing.
- A dual seven-segment LED display to provide you with a program number (eg P0) which indicates the current program of the isochronous data generator CPLD.
- The L41 Link chip is equipped with both M6 encryption / decryption blocks and an Elliptical Curve Accelerator (ECA) block to aid in node authentication. Or, alternatively, this board is equipped with an L40 Link chip having all features of the L41 part but without the M6 and ECA blocks.
- The Physical Layer IC (P21) block operates from a different power source than the rest of the card, and therefore may be powered from the 1394 cable, while the rest of the card is not powered. Provision also exists to power the entire board directly from the bus. A separate LED, labeled PHY Power, shows the status of Physical Layer power.
- A fully implemented isolation barrier system between the Link Layer and Physical Layer ICs may be enabled or disabled through switches S5 and S8. This system is used to demonstrate single capacitor isolation and proper PHY layer power supply design.

3 Hardware Design

This section contains a detailed description of each sub-section on the Evaluation Board. It also contains a troubleshooting section and recommendations for future 1394 designs, based on this reference design.

3.1 Hardware Description

A description of each sub-section of the board follows.

3.1.1 89C51 Memory Map

The 89C51 memory map shows the location of all the devices that may be accessed through the 89C51. The four items in the 89C51 memory map are the EPROM, the SRAM, the CPLD, and the PDI1394L41 registers. The layout of the map depends on whether software is being executed from (EP)ROM or flash ROM in the 89C51 MCU.

The PDI1394L41 registers are always mapped to start at the beginning of the last 2K of external memory. For this reason, only 62K of RAM are available for use, even though there are physically 64 K of RAM on the board. The memory maps are as follows:

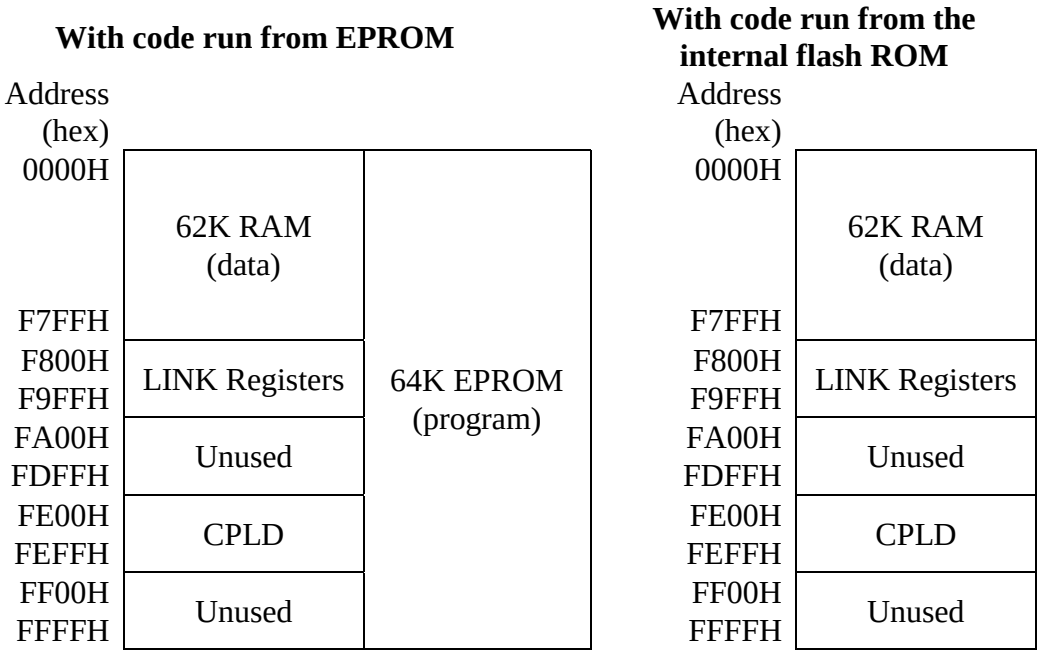


Figure 3-1: 89C51 microcontroller memory map

3.1.2 Software Memory Map

Address	Description
0000H-BFFEH	Code
BFFFH	ROM checksum
C000H-F7FFH	Data & variables
F800H-F9FFH	Link memory map
FFF8H-FFFCH	Node Unique ID serial number, lower 32 bits

Table 3-1: The Software Memory Map

3.1.3 Microcontroller Design

The 89C51RD microcontroller section is based on the standard 8051 design, using a latch for the lower eight address bits. For more details on this standard design, refer to Data Book IC20, 8051 Based Microcontrollers.

However, the flash programming process used for the 89C51 is unique as explained below.

3.1.3.1 Downloading a compiled program to the flash ROM in the 89C51 MCU

(This is an overview of the process, for complete programming details see the User's Manual)

It is necessary to start with a compiled 8051 program in Intel Hex format. This program will be loaded into a buffer within the WINISP software; the buffer contents subsequently will be downloaded into the 89C51 microcontroller unit on the RDK board. Any pre-existing program in the 89C51 must be erased before re-programming can be done. The WINISP software provides this function.

Programming steps:

CAUTION: Flash program mode is meant to be used ONLY with flash programmable microcontrollers labeled 89C51RD+ or 89C51RD2. Please make sure your MCU is one of these two types before proceeding.

WinISP is a utility that combines the power of in-system flash programming with the user friendliness of a graphical interface. WinISP requires Microsoft Windows (R) 3.0 or later and a free serial port. Following is a

short tutorial to demonstrate the use of the program.

1. Prepare the board, make sure the micro is firmly inserted into the socket. If you are using the Philips L41 RDK board, pin number 1 (upper side of the micro) should be facing the EPROM socket . Visually inspect the board for any damage or missing parts.

2. Connect a serial cable to the board and one of your PC's serial ports. Power up the ISP board.

3. Boot up your computer, start MS Windows and the WinISP software.

4. In WinISP, select the chip type, clock frequency (89C51RD+ / 22 MHz for Philips L41 RDK board) and the serial port number the board is connected to.

5. Force the micro into ISP mode. To do this, Place jumper JP7 in the position that shorts pins 1&2. The red LED (D12) will light to show program mode. Press and release the RESET button (S2) to initiate the program mode.

6. The system is now ready. You can use the buttons on the left of the WinISP window to load Intel hex files, program/erase/verify the part, set/reset the security bits etc.

7. After the MCU has been programmed, return the JP7 jumper to short pins 2&3. Also, please make sure that Dip Switch S1 (position 1) is in the "ON" position to run the code from the internal flash memory.

8. The micro can be reset at any time to run the program. Please note the following remarks:

   - The Boot Vector byte is used as a pointer to the ISP program. Unless a custom ISP program is present elsewhere in the Flash memory, this value should always be programmed to FCh.

   - Program the Status byte to 00h to execute your program after reset. To go back to ISP, simply continue from step 5. If the status byte is non-zero, the microcontroller will unconditionally jump to the address pointed to by the Boot Vector byte after a reset.

   - Do not program the lock bits; this will disable chip access by WinISP.

3.1.3.2 Interrupts

The host interface interrupt pin (pin 28) from the Link Layer IC (the PDI1394L4x), connects through a switch (see section 3.1.5: Evaluation Board Jumpers and Switches), to the 89C51 INT1 pin (U2-15). Since this is an open collector output from the Link IC, this line is also pulled-up with a resistor.

All interrupts generated by the Link Layer IC are multiplexed onto this line, and it is up to the interrupt service routine (ISR) in the 89C51 to determine the cause of the interrupt.

3.1.4 AV Data Simulator CPLD

U14 is the AV Data Simulator CPLD. It can be reprogrammed to perform many functions but is factory configured to generate pseudo digital video data in two formats, MPEG-2, and DVC. The data created by the CPLD can be directed to either AV port in order to be transmitted on the IEEE 1394 bus. The pseudo data is actually the output of a byte counter. The count starts at 00h for the first byte in each packet, and, depending upon which mode is selected, increases until a terminal count of BBh for MPEG-2, or DFh for DVC. The terminal count in each case is the number of the last byte in each mode, 188 bytes for MPEG, and 480 bytes for DVC. At the beginning of the next packet generated the count again increments from 00h. The CPLD is also capable of generating just the AV clock for a receiving node.

The bank of switches labeled S7 controls most functions of the CPLD. The CPLD is also connected to the 8051 MCU so that certain set-ups, commands, and data can be downloaded from the 8051 into the CPLD. The MCU can also read the CPLD. Other versions of the CPLD code will be available at the Philips 1394 website (*http://www.semiconductors.philips.com/1394/*) for downloading and use by RDK users; see the website for more information on this subject. The CPLD is Philips type PZ3128, and is in-system-programmable using the JTAG port connector labeled J11.

For the details of the setup of the CPLD using S7, refer to Section 3.1.5, Evaluation Board Jumpers and Switches, below.

> ***CAUTION:*** *Be very careful when enabling the transmit function of the AV Data Simulator. Enabling transmit while the Link Layer IC port is configured for receiving AV data can damage the Link Layer IC and the AV Data Simulator.*

3.1.5 Evaluation Board Jumpers and Switches

The 1394 Evaluation board has many jumpers and switches which allow you to change certain hardware settings. Below is an outline of the board, showing the location of these jumpers and switches.

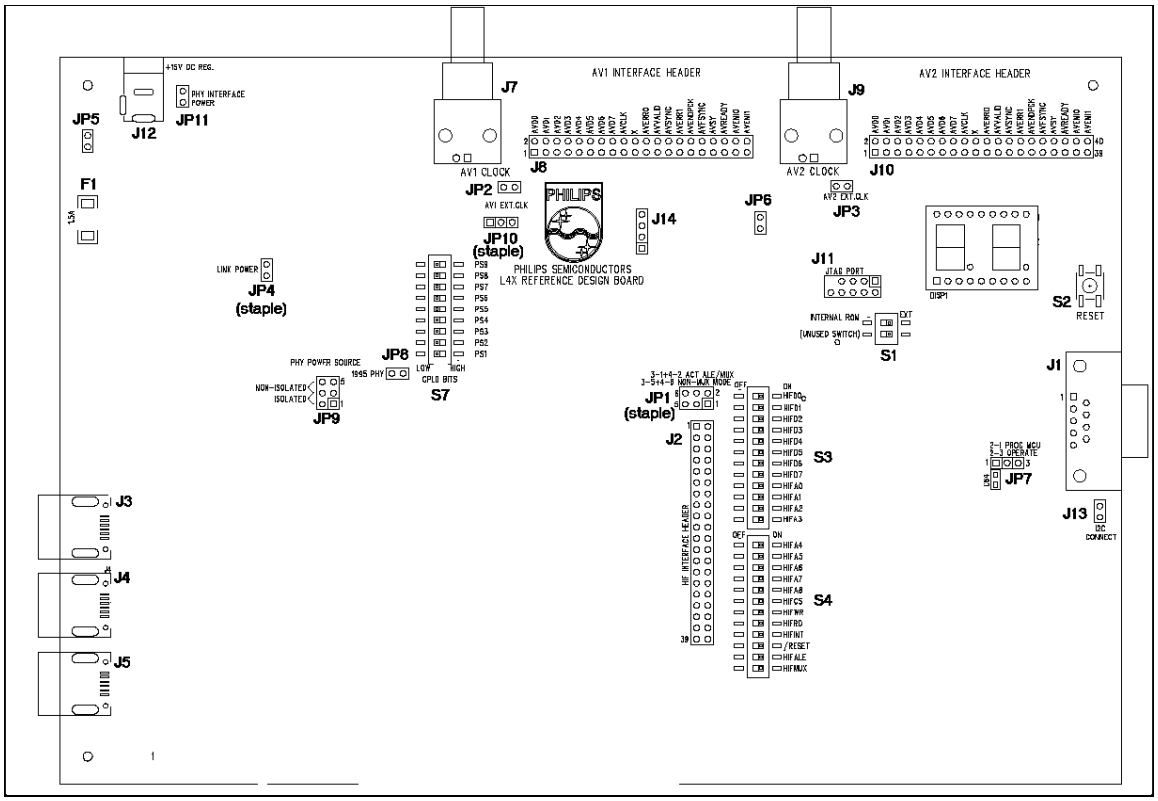


Figure 3-2: Locations of Evaluation Board Jumpers and Switches

The functions of these jumpers and switches are as follows:

Item	Description of functions
JP2	This jumper connects the AV1 clock output, AV1CLK, from the AV Data Simulator CPLD, to the AV1 clock input on the Link Layer IC. With the shunt in place, the AV Simulator will drive the line (when enabled). With the shunt removed, the AV1 clock, to the Link IC, may be driven by an external source, through J7 (see J7 below), or the link's internal clock may be used.
JP3	This jumper connects the AV2 clock output, AV2CLK, from the AV Data Simulator CPLD to the AV2 clock input on the Link Layer IC. With the shunt in place, the AV Simulator will drive the line (when enabled). With the shunt removed, the AV2 clock connection to the Link IC may be driven by an external source, through J9 (see J9 below), or the link's internal clock may be used.
JP4	Link Power Jumper: Used to disconnect the power from the link chip.
JP5	This jumper controls the power to the Physical Layer IC (the PDI1394P11). With the shunt in place, the IC (and associated circuitry) will be powered from the board power supply. With the shunt removed, the IC will only receive power if a 1394 cable, capable of supplying power, is attached.

JP6	CPLD Clock Jumper: Used to disconnect the clock output generated by U16 from the CPLD.
JP7	Microcontroller programming jumper: Used to put the microcontroller into flash programming mode. Normal operation of the MCU is obtained with the jumper in position over pins 2 and 3. When the jumper position is changed to short pins 1 and 2 together, the MCU enters flash programming mode after the reset button is pushed and released.
JP8	"1995 PHY" jumper: The Physical Layer chip provided with this RDK board is the PDI1394P21. This PHY conforms to the 1394A standard of operation. Had this board been fitted with a PHY which conforms ONLY to the 1394-1995 standard, this jumper would have been shorted (with a staple), telling the Link chip that the fitted PHY is a 1995 (only) compliant part.
JP9	Isolated /Non-isolated jumper block: This jumper block (2 jumpers required) selects whether the PHY ground and power domains of the board are (a) directly coupled to the link ground and power domain, or (b) isolated from the link ground and power domain. The board is shipped in the directly coupled (non-isolated) configuration with one jumper shorting pins 3 and 5 while the other shorts pins 4 and 6 of the jumper block. To use the board in isolated mode, it is necessary to short pins 1 to 3 and 2 to 4.
JP10	Flash programming voltage selector: This jumper selects either 12v or 5v programming voltage level for the programming voltage used to flash program the MCU. The factory setting of this jumper (staple) is shorting pins 1 and 2... this provides 12v programming voltage used for programming 89C51RD+ type MCUs. 89CRD2 type microcontrollers require only 5v for flash programming, so that type of microcontroller will use a jumper/staple to short pins 2 and 3.

Table 3.2 Jumper Descriptions

Item	Description of functions
S1	Switch 1 of this pair of switches controls whether the 89C51 will execute code from internal ROM (with the switch off) or from the external EPROM (with the switch on, as marked on the board). Switch 2 of this set is reserved.
S2	This is the reset button for the board. Pressing this button will reset the 89C51, causing it to start executing code from internal ROM or the external EPROM, depending on the position of S1. This button also resets the Link and Physical Layer IC's.
S3, S4	These switches control the connectivity of the Host Interface, between the 89C51 and the Link Layer IC, so that all or part of the interface may be controlled by an external source. With all switches on, the interface is fully connected. If you wish to disconnect some or all of the host interface signals, set the switches off, according to the following diagram:

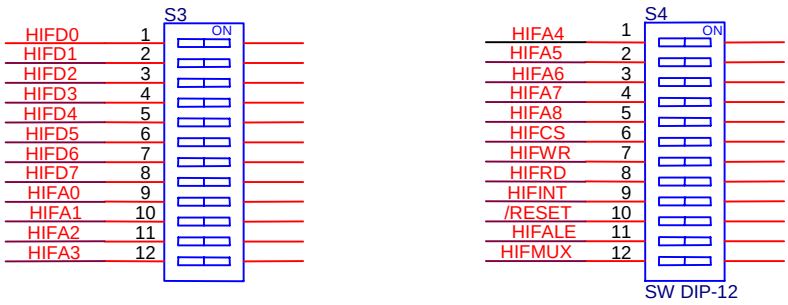


Figure 3-3: Host interface interconnectivity switches

Once the lines of interest have been disconnected, you may control them through the Host Interface Header (J2). See Section 3.1.7: Evaluation Board Headers and Connectors for more information.

S6 These switches control the status of the bits PC3-0. and "C" into the Physical Layer IC. Which switch controls which bit is marked above the switch, on the board. A switch in the HI position corresponds to a 1, and LO corresponds to a 0, as marked on the board. For more information on these bits, see the associated Physical Layer IC documentation.

Switch section 5 on this switch is not used.

S7 This set of switches sets the options for the AV Data Simulator CPLD. The switches are marked PS1 through PS9.

PS9 Switch PS9 controls the receive / transmit function of the CPLD. When this switch is set to 0 (LO), the device will be in receive mode. All lines will be tri-stated (except clock when PS4 = 1). When this switch is set to 1 (HI), the CPLD will be in transmitting mode, and will send out data, synchronous with its clock. When PS9 is in its active state the lighted decimal point on the LED display will indicate to which port the CPLD sends data; this should be the active transmit port of the Link chip. Switch PS7 selects the port.

PS8 Switch PS8 controls the MPEG-2/DVC mode. When this switch is 1 (HI), the device will transmit MPEG-2 size packets (188 bytes). When this switch is 0 (LO), the device transmits DVC packets of 480 bytes.

PS7 Switch PS7 directs the generated packets to the proper AV port. When this switch is in the 1 (HI) position, the packets are directed to AVport1. In the 0 (LO) position, the packets are directed to Avport2. The position of the lighted decimal point on the LED display indicates to which port the CPLD signal is directed; left to AV port1, right to AV port2.

PS6 Switches PS6 and PS5 are used to select the clock frequency. When these
PS5 switches are set to 11, 10, 01, 00 then the clock frequency is 0.125, 0.25, 0.5 or 1 times the U16 clock frequency; multiply by the input clock respectively:

Switch PS6	Switch PS5	Clock Rate (MHz)	Data Rate (peak) (MB/s)
0	0	20.0	160
0	1	10.0	80
1	0	5.00	40
1	1	2.50	20

PS4 Switch PS4 is used to supply a clock (only) to a receiving AV port when it is placed in the HI position while PS9 is in the receiving (LO) position. Note, switch PS9 takes precedence over PS4 when PS9 is in transmit (HI) position. When PS4 is in its active state the lighted decimal point on the LED display will indicate to which port the receive clock is directed; this should be the active receive port of the Link chip. Switch PS7 selects the port.

PS3 Switches PS3 to PS2 are not used in this rendition of the CPLD program.

PS2 The factory programmed CPLD is fitted with program 0 indicated by P0 on this display when switch 1 is in the hi position.

PS1 Switch PS1 is used to indicate the program number in the CPLD. For further information about the CPLD and its options, see the Xilinx web site on the Internet at www.xilinx.com.

WARNING: *Do not put the AV Data Simulator CPLD in transmit mode, unless the Link Layer IC port is configured to transmit. Enabling the CPLD's transmit mode at any other time can damage the Link Layer IC and the CPLD*

S5, S8 These switches enable or disable the isolation barrier between the Physical and Link Layer ICs. Moving all of the switches to the ON position disables the isolation barrier, and moving all of to the OFF position enables the barrier, as marked on the board. Please note that all switches must be in the same position, either ON or OFF. For more information, see the section 3.1.10: Isolation Barrier.

Table 3.3 Description Of Switches

3.1.6 Default/Factory Switch and Jumper Settings

S1	ON (External ROM)	**S7**	all LOW; put PS0 HI to show program number of CPLD on the display
S2	Reset (off)	**JP1**	Jumper 3-5 and 4-6 (Non-Mux mode)
S3	1 to 12 all ON (enabled)	**JP2 to JP6, JP10**	All fitted with jumpers
S4	1 to 12 all ON (enabled)	**JP7**	Jumper 2 –3 (Operate)
S5 & S8	All "Not Active" (ON)	**JP9**	Jumper 3-5 and 4-6 (Non-Isolated)
S6	PC0 - "C" all LOW	**JP11**	Open, no jumper

Table 3-3: Default/Factory Switch and Jumper Settings

3.1.7 Evaluation Board Headers and Connectors

Below is a description of all the headers and connectors on the Evaluation Board. Please see Figure 3-2: Evaluation Board Jumpers/Switches to determine the location of each.

Item	Description
J1	This is the serial connector for the board. The 9-pin connector allows a standard serial cable, NOT a null-modem cable, to connect the board to a standard PC serial port. Note: the cable included with the kit will allow a direct connection to a PCs 9-pin serial port. To connect to a 25-pin serial port, the 9-pin to 25-pin adapter, included in the kit, may be used.
J2	This header connects to the host interface of the Link Layer IC. The pin-out is as follows:

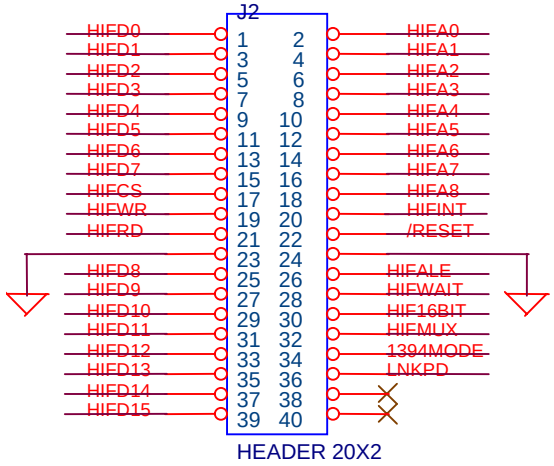


Figure 3-4: Host interface header

J2 (cont) You may use this header to monitor or drive any of the host interface signals. However, if you drive a signal, you must first disconnect that signal from the 8051, using S3 and/or S4.

J3, J4, J5 These are the 1394 cable connectors. It does not matter how many, or in what order they are used. However, when connecting multiple boards together, be sure that a loop is not formed (i.e. there should not be a circular path, returning to a board).

J6 Link-PHY Interface Test Header. Used to look at signals between the Link and PHY chips. The pin-out is as follows:

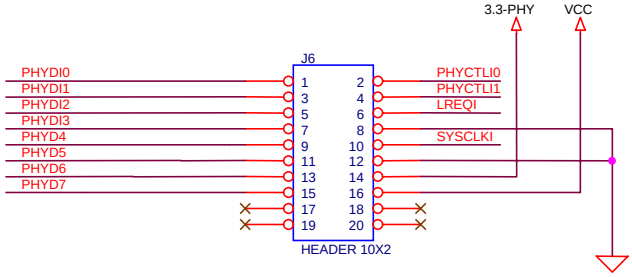


Figure 3-5: Link-PHY Interface Test Header

J7 This BNC connector can be used to supply an external AV1 clock to the Link Layer IC. If it is used for this purpose, the shunt at JP2 must be removed. Otherwise, this connector can be used to monitor the AV1 clock produced by the AV Data Simulator CPLD.

J8 This header connects to the AV1 interface of the Link Layer IC. Please note that the names of the pin functions on the board appear on the ODD side of the header while they refer to EVEN numbered pins. The pin-out is as follows:

CAUTION: *Before driving any of the signals, you* ***must*** *ensure that the particular port of the Link Layer IC is configured as an input (to transmit AV data on the 1394 bus) or* ***it may be damaged.***

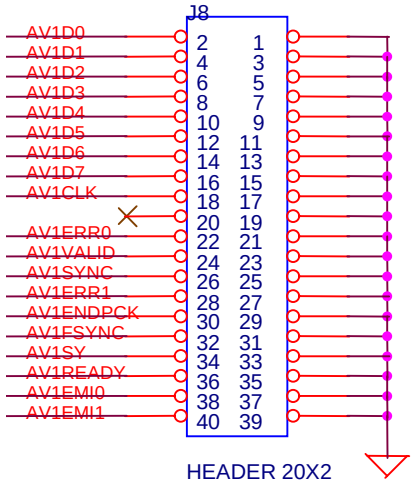


Figure 3-6: AV1 Interface Header

J9 This BNC connector can be used to supply an external AV2 clock to the Link Layer IC. If it is used for this purpose, the shunt at JP3 must be removed. Otherwise, this connector can be used to monitor the AV2 clock produced by the AV Data Simulator CPLD.

J10 This header connects to the AV2 interface of the Link Layer IC. Please note that the names of the pin functions on the board appear on the ODD side of the header while they refer to EVEN numbered pins. The pin-out is as follows:

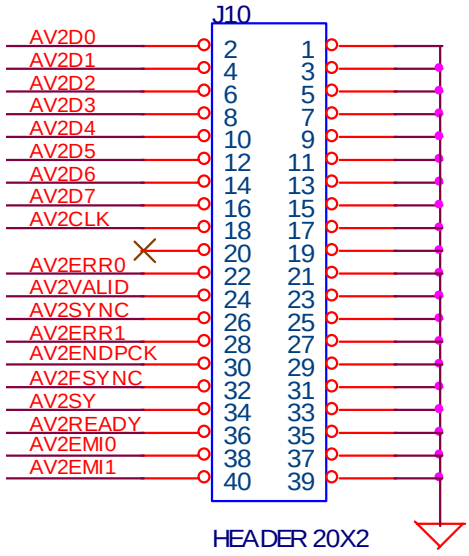


Figure 3-7: AV2 interface header

J10 (cont) You may use this header to monitor or drive the AV2 interface signals. However, if you wish to drive the AV signals, using this header, you must first put the AV Data Simulator (U14) in a high-impedance state by placing S7 switch PS8 and PS3 in the LO position.

J11 This Reference Design Board is equipped with a data simulator CPLD that can be erased and re-programmed In-System. J11 is a JTAG interface to the CPLD (U14) for this purpose. A special cable is connected between the printer port of a PC and J11. Using software supplied by Xilinx, the CPLD can be erased and re-programmed with programs written using Philips XPLA Professional or the XILINX CPLD programming system. Consult the Xilinx Website for CPLD programming instructions.

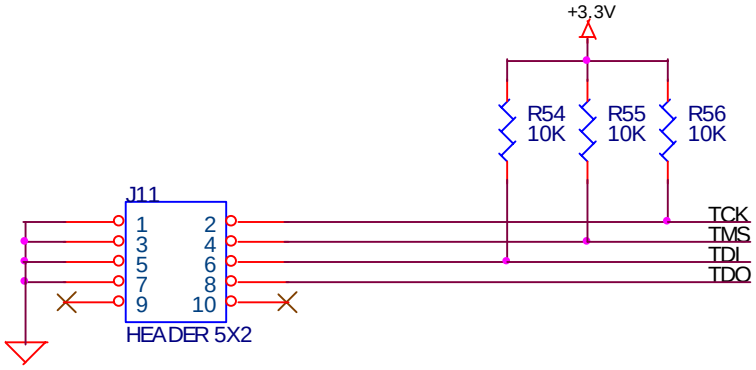


Figure 3-8: JTAG Interface for CPLD Programming

J12 This is the power connector (2.0mm center positive). A $12V_{DC}$, unregulated power supply (provided with the kit), plugged into this connector, provides power to the board.

J13 If the 8051 microcontroller is replaced with an 80C654, or similar microcontroller, the I^2C interface to the microcontroller can be accessed through this header. Pin 1, marked with a dot on the board; connects to Port 1, pin 6, which is the SCL pin. Pin 2 connects to Port 1, pin 7, which is the SDA pin.

3.1.8 EPROM Socket

U9 is a socket containing an EPROM. The EPROM shipped with the kit is a 64K x 8, 90 ns EPROM, containing the loader and IEEE 1394 driver. However, any standard 27C512 (see the schematics for the exact pin-out) 64K x 8 EPROM, with an access time less than 120 ns may be used (assuming a 22.118 MHz MCU clock oscillator frequency).

If a different EPROM is used, the new code must be compiled, linked, and loaded into the EPROM so that is starts at address 0000H.

3.1.9 Processor Clock Oscillator

U1 is a standard 22.118 MHz surface mount packaged oscillator chip. However, if you wish to try the board at different frequencies, you may replace an oscillator with the frequency of your choice, within the specified limits (3.5 to 24MHz). Any oscillator speed may be used, as long as it is within the requirements for the speed grade of the 89C51 (currently 3.5 to 24MHz). Please note that if a different frequency is used, the RS-232 communications may not function properly, unless the code in the EPROM is re-compiled to take into account the new frequency. The default frequency of 22.118MHz was chosen since it divides evenly into standard serial port speeds.

3.1.10 Isolation Barrier

An isolation barrier is set up between the Link Layer IC and the Physical Layer IC. This barrier is implemented by placing a 0.001µF capacitor in series with every line that connects the Link IC to the Physical Layer IC. The switches in the banks labeled S5 and S8 can de-activate this barrier by short circuiting these capacitors. The normal mode of operation of the RDK board is with the capacitors shorted (non-isolated mode).

As well, when the switches in S5 are moved, the levels on the pins, on the Link IC and Physical IC, that set if an isolation barrier is present, are changed. Therefore, all the switches labeled D7 through RESET on S5 and S8 **must** be in the same position, either

all toward NOT ACTIVE (to disable the barrier) or all toward ACTIVE (to enable the barrier). Please note: There are power supply considerations when using isolation, please see the section on ISOLATION POWER when activating isolation

3.1.11 Using Galvanic Isolation

Please note: configuring the board to operate in Galvanic isolation mode should be accomplished ONLY with the board power OFF. Disconnect the power supply first!

This RDK board is equipped with a fully isolated PHY ground and power domain which can be used to demonstrate and test the L4x and P21 in full Galvanic isolation mode. The ground and power planes of the link and PHY are separated, that is, the link has it's own Link power plane and ground plane. The PHY power and ground planes are located under the PHY chip and its associated components. The two ground planes are tied together under switch S5 (denoted by GND switches). The PHY and link ground planes are also tied together at jumper JP3 also (to connect the PHY ground plane to a non-isolated 3.3v PHY power supply). If these jumpers are removed the link and PHY ground planes are separated by a resistor capacitor isolation network (100 nF in parallel with a 10 nF capacitor, in parallel with a 1 Meg Ohm resistor, per IEEE 1394). Please see the schematic diagram, page 5, provided in the back of this manual. This network of parts is located under S5 and provides ground return path for the signals which flow between the L4x and the PHY chip. Isolated power is provided to the PHY by means of the isolating dc to dc converter and is connected to the PHY by means of jumper set JP3 which also selects the output ground of the converter for the PHY ground. To complete the set-up of isolation it will be necessary to move all switches of the S5 and S8 dip switches to the "ACTIVE" (off) position. This action removes the short circuits placed across the isolation capacitors in the link-PHY interface and allows them to work as low "high pass" circuit components (See App Note 2452 for more details). All of the above steps MUST be done in order for Galvanic isolation to work; omission of any step will cause mis-operation of the isolation mode and could possibly cause node malfunction or component damage.

Please refer to Application Note 2452 for operation of the RDK in isolated mode. If you are unsure of the use or need for Galvanic isolation we recommend that you read the introductory section of that application note.

To change the board operation back to the direct connect mode (factory supplied mode of operation) please remove the power from the board and reverse all steps indicated above.

3.1.11.1 Overview

One of the CPLDs (U5) on the board performs various decoding and housekeeping functions. This CPLD is a PZ5032, 32 macrocell device in a 44 pin PLCC package. It is fitted to a socket and may only be re-programmed in a device programmer.

U5 handles data transfer to/from the data simulator CPLD. It decodes the CPLD at address FE00h.

U5 is also used as an address decoder, to generate all the chip select and read/write signals for the SRAM, EPROM, and Link Layer IC.

3.1.11.2 HDL Code for U5

If it becomes necessary to use or modify the code for U5, please contact Philips Semiconductors applications engineering department at 1394@philips.com for assistance.

3.1.12 LEDs

The Evaluation Board has several LEDs on its top surface, to inform you of certain conditions and events. See Section 3.1.5: Evaluation Board Jumpers and Switches for the locations of the LEDs.

The function of each LED is listed here. The function of each is also marked on the board, with the label that is in quotes below.

LED	Description of function
D1	User Program – This LED will light when a user program is being executed by the 89C51 if the user codes the 89C51 to do this function. A user program is one that has been downloaded through the serial port by the WINISP software.
D2	User – This LED is controlled by port 1, bit 3 of the 89C51. Its purpose is simply to give you feedback, and may be used in any way you see fit in your application. A logic 1 on port 1, bit 3, which is its default after an 8051 reset, will light the LED. A logic 0 will turn off the LED. By default this LED flashes in a heartbeat pattern when the RDK is running smoothly, and switches to a "Blink Code" on a fatal error. "Blink Codes" are documented in the *User's Manual*.
D3	Link Access – This LED lights when the 89C51 accesses the Link Layer IC through the host interface. ***Note:*** *As these accesses are so short in duration, it is sometimes difficult to see the LED flash, even though accesses are taking place.*
D4	Cable Active – This LED, beside the 89C51 socket (U2), lights when an active cable is plugged into any one of the three 1394 ports (J3, J4, or J5). In order for the cable to be active, the other end must be plugged into a live 1394 port. For

LED	Description of function
	the LED to light, there must also be power to the Physical Layer section of the board (see D8 below).
DISP	LED display – Multifunctional – Function depends upon which program is loaded into the CPLD. See Section 3.1.5: Jumpers and Switches for more information.
D7	+3.3V – This LED lights when the 3.3V power is active on the board. 3.3V is used by the CPLD, the Link Layer IC, and all of its associated circuitry. 3.3V is also used by the Physical Layer IC; however, it uses a different power source (see PHY PWR below).
D6	+5V – This LED lights when the 5V power is active on the board. 5V is used by the 89C51 and its associated circuitry
D8	PHY PWR – This LED lights when the Physical Layer ICs power is active (a 3.3V power source).

Table 3-4: LEDs and Descriptions

3.1.13 Test Points

There are several test points on the card to facilitate test probe connection to many of the Physical Layer IC signals. Each test point is a plated hole, with a label.

The following is a list of all the test points. For a description of each signal, please see the associated *Physical Layer IC* documentation.

Test Points	Labels	Test Points	Labels	Test Points	Labels
TP1	CLK50	**TP10**	TPB2-	**TP19**	LINKPD
TP2	TPA1+	**TP11**	TPBIAS2	**TP20**	PBRST
TP3	TPA1-	**TP12**	TPA3+	**TP22**	PSEN
TP4	TPB1+	**TP13**	TPA3-	**TP23**	U5-38
TP5	TPB1-	**TP14**	TPB3+	**TP24**	U5-39
TP6	TPBIAS1	**TP15**	TPB3-	**TP25**	ALE
TP7	TPA2+	**TP16**	TPBIAS3	**TP26**	U10-1
TP8	TPA2-	**TP17**	HIFWAIT	**TP27**	U10-21
TP9	TPB2+	**TP18**	P3.2	**TP28**	U11-1
TP29	U11-21	**TP30**	CYCLEOUT		

Table 3-5: Test Points and Labels

3.1.14 Prototyping Area

In the bottom center of the Evaluation Board is the Prototype Area.

All the holes in the center grid are plated, but not connected to anything. For prototyping, extra components may be placed, and soldered, in this area, and connected together, or to other parts on the board, by way of external wires.

All the holes in the bottom rail, below the center grid, labeled PHY GND and LINK_GND are connected to the ground planes. They may be used to connect to components in the prototype area. Similarly, there are three power rails, a +5V, a PHY +3.3V and a LINK +3.3V, above the center grid. Care should be taken not to connect any of these holes directly to ground. Also, note that the LINK +3.3V rail is connected to the same voltage regulator used to power the Link Layer IC (and the +3.3V LED) and not to the Physical Layer (PHY) ICs power. The PHY has two power sources available, isolated and non-isolated, the proper supply must be used dependent upon use of isolation or not.

The hole pattern shown as J14 is connected to unused pins on the AV Data Simulator CPLD, and may be used as inputs/outputs for user defined versions of the CPLD program. Until that time however, these holes should remain disconnected.

3.1.15 Power Issues

The 1394 AV Evaluation Board was designed with different power supplies for both the Link and Physical layer sections. In this configuration, the Physical Layer section may be powered solely from the 1394 cable, acting as a repeater, while the 89C51 and Link Layer remain unpowered. The Physical Layer IC monitors the power to the Link Layer IC (through its Link Power Status pin), and will act as a repeater only, if it 'sees' that there is no power to the Link Layer.

Unfortunately, this system of multiple power supplies is not automatically configured. When the JP5 has a shunt in place, the Physical Layer power supply is driven by the 15V supply. This shunt must be in place if the board is to be fully powered from its 15V supply. The shunt must be removed if the Physical Layer is to be powered from the 1394 cable, with the 89C51 and Link Layer operating from the 15V supply.

The Physical Layer power supply also contains a current limiting, self-resetting, fuse (F1). If the current drawn by the Physical Layer section, and any other Physical Layer sections powered from that card (through the 1394 cable), goes above 1.5 A, the fuse will trip. If this happens, disconnect all power supplies from the system, and wait for the fuse to cool down, at which point the fuse will reset. When re-connecting the boards, ensure that there is a smaller load placed on a single Physical Layer power circuit.

3.2 Troubleshooting

Problem	Corrective Action
+3.3V and +5V LEDs do not light.	Check that the 15V-power supply is properly plugged in to the card at J12 and plugged in to an active AC power source.
PHY PWR LED does not light.	If the board is to be powered from its 15V-power supply, check that a shunt is in place on JP5. If it is not, check that a 1394 cable, capable of supplying power, is connected to one of the ports.

CABLE ACTIVE LED does not light.	Check that the PHY PWR LED is lit. The Physical Layer must have power for the Cable Active LED to light. Check that a 1394 cable is plugged in to one of the ports, and that the other end of the cable is plugged in to another active 1394 device.
Communications between host computer and board not functioning.	Check that there is a serial cable connected between the board (J1) and host computer. Check that the cable being used is a serial cable, and not a null modem cable. The cable shipped with the kit is the proper cable to use.
Code is not being executed from a user programmed EPROM.	Check that the EPROM is fully inserted (all pins in the socket) and that pin 1 is up (according to the board markings). Check that switch 1, on S1, is ON (meaning External PROM). Check that when the code was compiled, linked, and loaded into the EPROM, it was always set to start at address 0000H.

Table 3-6: Troubleshooting Problems and Corrections

4 Customer Support

Philips Semiconductors is committed to giving you, our customer, the best possible technical support. If your system appears to be functioning incorrectly, please attempt a self-diagnosis with the help of the Troubleshooting section, Chapter 9 of the Software Users Manual.

If you are still having trouble, please follow these steps before contacting our technical support teams:

1. Be sure to read the relevant sections of the documentation. Many times the answer is right there.
2. Document the problem you are experiencing. Be as specific as you can. It is also useful to know the following:
    a. The RDK board serial number;
    b. Your operating system release version; and, if applicable
    c. Settings used during software compilation
    d. Settings of the RDK board jumpers and switches

For assistance on Philips Semiconductors A/V Link Layer Controller (PDI1394L41) or the Physical Layer Interface (PDI1394P11A), please contact:

your local Philips sales representative

or send email to: 1394@philips.com

5 Glossary

The various acronyms, abbreviations, and special terms used frequently in this manual are here defined for convenient reference.

1394	A fast external serial bus standard originally developed by Apple under the name FireWire. Other names for this technology include I-link, and Lynx.
8051	A standard, low cost, microprocessor; 89C51 is a derivative part.
AV	Audio/Video
CMC	Configuration Manager Capable or PHY "C" bit
CPLD	Complex Programmable Logic Device
DVC	Digital Video from a camcorder
EPROM	Erasable Programmable Read-Only Memory
PZ5032	A programmable logic device, 32 macrocell
PZ3128	A programmable logic device, 128 macrocell
PHDL	Philips Hardware Description Language, a superset of computer languages used to program Field Programmable Gate Arrays and Programmable Logic Devices
IC	Integrated Circuit
I^2C	Inter-IC, a bus developed by Philips Semiconductors used to connect integrated circuits.
IEEE	Institute of Electrical and Electronic Engineers
ISR	Interrupt Service Routine
LED	Light Emitting Diode
MB/s	Megabytes per second
MPEG-2	A high compression isochronous format, commonly seen in satellite TV, video cameras, and DVD players.
PHY	Registers of the PDI1394P21 3-port physical layer interface, 400 Mbps.
PDI1394L4x	Identifier of the link chip which handles transactions between 1394 boards. The PDI1394L41 Philips Semiconductors 1394 Full Duplex Content Protection Audio/Video Link Layer Controller is an IEEE 1394a compliant link layer controller featuring an embedded AV layer interface. The AV layer is designed to pack and unpack application data packets for transmission over an IEEE 1394 bus using isochronous data transfers. It runs at 49.978MHz and uses a 3.3V power supply.
PDF	Portable Document Format
RAM	Random Access Memory
RDK	Reference Design Kit
Registers	A high speed data storage area within a CPU.

ROM	Read-Only Memory
RS-232	A standard interface for connecting serial devices.
SRAM	Static RAM
VCR	Video Cassette Recorder
Win32	The Microsoft Windows API for developing 32-bit applications.
Win9x	The Microsoft Windows 95 or 98 operating system.

Appendix A: Bill of Materials

The following is the original Bill of Materials (BOM) for the board. However, for reasons of cost and availability, some parts may have been substituted during manufacturing.

1394L4x AV Link Evaluation Board.

Item No.	Qty	Manufacturer Part Number	Mfg. Name	Part Reference	Description	Vendor	Vendor Part #
1	32	C0805C104M5UAC	KEMET	C1,C2,C3,C4,C6,C7,C8,C10,C11,C12,C13,C14,C15,C16,C17,C18,C19,C20,C39,C40,C41,C42,C43,C44,C45,C46,C47,C48,C51,C59,C60, C64	Capacitor 0.1 uF 20 % 50 V Size 0805	Newark	92F5747
2	2	ECE-V1HA220UP	PANASONIC	C54, C56	Capacitor 22uF 50v D Case Electrolytic	Digikey	PCE3194CT-ND
3	18	C0805C102K5RAC ECU-V1H102JCX	KEMET PANASONIC	C9,C23,C24,C25,C28,C29,C30,C31,C36,C65,C66,C67,C69,C70,C71,C72,C73	Capacitor, 1nF 10 % 50 V Size 0805	Newark DIGIKEY	93F2383 PCC102CGCT-ND
3A	1	ECU-VIH103KBG	PANASONIC	C49	Capacitor, 10nF 10 % 50 V Size 0805	Digikey	PCC103BNCT-ND
4	3			C26,C33,C37	Capacitor 270 pF 5 % 50 V Size 0805		
5	4	ECE-V1HA010R	PANASONIC	C5,C27,C34,C38	Capacitor 1 uF 50 V B Case Electrolytic	Digikey	PCE2022CT-ND
6	2	ECU-V1H220JCN	PANASONIC	C32,C35	Capacitor 22 pF 50 V 5 % Size 0805	Digikey	PCC220CNCT-ND
6A	1	ECE-V1AA101UP	PANASONIC	C61	Capacitor 100 uF 10 V D Case Electrolytic	Digikey	PCE2039CT-ND
7	3	T491D107K010AS	KEMET	C52,C53,C58	Capacitor 100 uF 10 V D Case Tantalum	Newark	
8	1	ECE-V1HA100P	PANASONIC	C50	Capacitor 10 uF 50 V D Case Electrolytic	Digikey	PCE2033CT-ND
9	3	HSMS-C650	HEWLETT PACKARD	D1,D2,D12	LED RED Surface Mount	Newark	06F7032
10	2	HSMG-C650	HEWLETT PACKARD	D3,D4,	LED GREEN Surface Mount	Newark	06F6955
11	3	HSMY-C650	HEWLETT PACKARD	D6,D7,D8	LED YELLOW Surface Mount	Newark	06F7123
12	3	MBRS1100T3	Motorola	D5, D9, D11	Schottky Rectifier, 403A Case SMB	Newark	06F9801
13	1	DL4007	VISHAY LITEON	D10	General Purpose Rectifier Case MELF	Digikey	1N5818MCT-ND
14	1	SMD075-2	RAYCHEM	F1	Resettable Fuse).75 A hold 1.5 A trip	Digikey	SMD075CT-ND
15	3	8532-30LTR	DELEVAN	L1,L2,L3	Inductor 270 uH Size 8532	Digikey	DN3230CT-ND

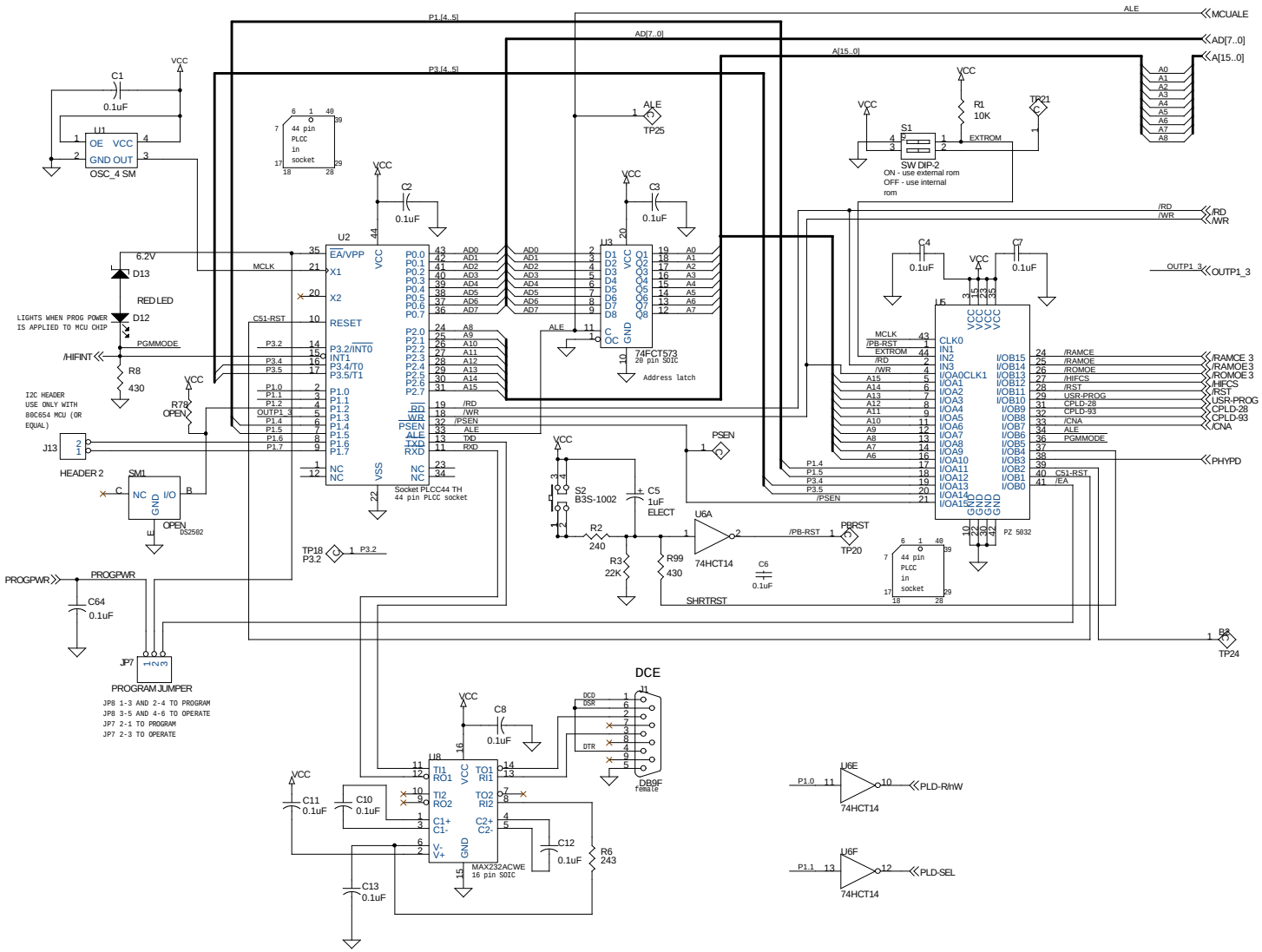
16	21	RC11J10K0	PHILIPS	R1,R9,R11,R12,R13,R31, R33, R36,R44,R45,R46,R47,R48,R49,R50,R51,R52,R54, R55,R56,R81	Resisor 10 k ohm 1/10 watt 5% Size 0805	Digikey	P10.0KCCT-ND
17	5	RC02H243R	PHILIPS	R2,R6,R7,R74,R77	Resistor 243 ohm 1/10 watt 1% Size 0805	Digikey	P243CCT-ND
18	4	RC11J1K00	PHILIPS	R10,R37,R76,R102	Resistor 1.0 k ohm 1/10 w 5% Size 0805	Digikey	P1.00KACT-ND
19	1	RC02H100R	PHILIPS	R15	Resistor 100 ohm 1/10 w 1% Size 0805	Digikey	P100CCT-ND
20	1	RC02H392K	PHILIPS	R106	Resistor 392 k ohm 1/10 w 1% Size 0805	Digikey	P392KCCT-ND
21	12	RC02H56R2	PHILIPS	R22,R23,R25,R26,R28,R29,R34,R35,R38,R39,R41, R42	Resistor 56.2 ohm 1/10 w 1% Size 0805	Digikey	P56.2CCT-ND
22	3	ERJ-8ENF5.11K	PANASONIC	R24,R30,R40	Resistor 5.11 k ohm 1/10 w 1% Size 0805	Digikey	P5.11KCCT-ND
23	1	ERJ-8ENF6.34K	PANASONIC	R27	Resistor 6.34 k ohm 1/10 w 1% Size 0805	Digikey	P6.34KCCT-ND
24	2	RC02H1M00	PHILIPS	R19,R88	Resistor 1 meg ohm 1/10 w 1% Size 0805	Digikey	P1.00MCCT-ND
25	16	RC11J180R	PHILIPS	R57,R58,R59,R60,R61,R62,R63,R64,R65,R66,R67, R68,R69,R70,R71,R72	Resistor 180 ohm 1/10 w 5% Size 0805	Digikey	P182ACT-ND
26	7	ERJ-6GEYJ430	PANASONIC	R4,R5,R8,R43,R73, R108,R189	Resistor 432 ohm 1/10 w 1% Size 0805	Digikey	P432CCT-ND
27	3	ERJ-6GEYJ2.0K	PANASONIC	R20,R53,R103	Resistor 2.0 K ohm 1/10 w 1% Size 0805	Digikey	P2.0KACT-ND
28	6	ERJ-6GEYJ22K	PANASONIC	R3,R75,R79,R80,R86,R87	Resistor 22.0 K ohm 1/10 w 1% Size 0805	Digikey	P22KACT-ND
29	0	RC11J4.7KR	PHILIPS	R78	Resistor, 4.7K ohm, 1/10w 5% Size 0805	Digikey	P4.7KACT-ND
30	2	752-18-1-223-G	CTS	RN1,RN2	Resistor Network 22 k ohm Dual Row	Allied	745-0760
31	1	219-2MST	CTS	S1	Dip Switch 2 circuit Surface Mount	Digikey	CT2192MST-ND
32	1	B3S-1002	OMRON	S2	Pushbutton Switch	Digikey	SW416-ND
33	3	219-12MST	CTS	S3,S4,S5	Dip Switch 12 circuit Surface Mount	Digikey	CT21912MST-ND
34	2	219-5MST	CTS	S6, S8	Dip Switch 5 Circuit Surface Mount	Digikey	CT2195MST-ND
35	1	219-9MST	CTS	S7	Dip Switch 9 Circuit Surface Mount	Digikey	CT2199MST-ND
36	2	PCS-044SMU-11	AUGAT	SOCK 1, SOCK 2	44 pin PLCC Socket	Newark	91F2768
37	1	CY74FCT573TSOC	CYPRESS	U3	Octal Latch		
38	1	DL35 6.2V +/- 5% SMD	VISHAY LITEON	D13	6.2 V Zener Diode	Digikey	ZMM5234BCT-ND
39	1	MC74HCT14AD	MOTOROLA	U6	Hex Schmitt Trigger Inverter	Newark	07F6877
40	4			P8, P9, P10, P11	Wire Staple, .1 inch, #22 AWG	Newark	

41	1	MAX232ACWE	MAXIM	U8	Dual RS-232 Transceiver	Digikey	MAX232ACWE-ND
42	2	CY7C195-15VC	CYPRESS	U10,U11	64 K x 4 15 nsec SRAM	Future	CY7C195-15VC
43	1	IC149-144-045-S5	YAMAICHI	SOCK 4 Not for use in production units	144 Pin LQFP Test Socket	Yamaichi	IC149-144-045-S5
44	1	PDI1394P21	PHILIPS	U13	Philips Phy IC	Philips	PDI1394P21
45	1	XCR 3128A-7VQ100C	XYLINX	U14	CPLD, 128 Macrocell, 3volt, 5V tolerant	XYLINX	XCR 3128A-7VQ100C
46	1	SG-636PCE-20.000MC2	EPSON	U16	20 Mhz 3 - 5V Oscillator Surface Mount	Digikey	SE2833CT-ND
47	1	MA-506-24.576M-C2	EPSON	Y1	24.576 Mhz Crystal	Digikey	SE2638CT-ND
48	1	LDD-A512RI	LUMEX	DISP 1	Dual LED Display Green Common Anode 0.56"	Digikey	67-1456-ND
49	1	44N8882	SPC	J1	DE-9 PCB Mount RS-232 Socket	Newark	44N-8882
50	1	PTC3SFAN	Sullins	JP7	1 x 3 .1" header	Digikey	S1212-3-ND
51	1	PTC3DFAN	Sullins	JP9	3 x 2 .1" dual row header unshrouded	Digikey	S2212-3-ND
53	3	53462-0611	MOLEX	J3,J4,J5	1394 Connector PCB Mount Right Angle, Flat	Digikey	WM17300-ND
54	1	PTC10DFAN	Sullins	J6	20 Pin Dual Row Header .1" Unshrouded	Digikey	S2212-10-ND
55	2	227161-9	AMP	J7,J9	BNC Connector PCB Mount Right Angle Jack	Allied	512-2179
56	3	PTC20DFAN	Sullins	J2, J8, J10	40 Pin Dual Row Header .1" Unshrouded	Digikey	S2212-20-ND
57	1	PTC5DFAN	Sullins	J11	10 Pin Dual Row Header .1" Unshrouded	Digikey	S2212-5-ND
58	1	PJ-002A	CUI STACK	J12	Male Power Jack Closed 2.0 mm	Digikey	CP002A-ND
59	4	PTC2SFAN	Sullins	JP2,JP3,JP5,JP6	2 x 1 .1" header	Digikey	S1212-2-ND
60	8		3M	P1,P2,P3,P4,P5,P6,P7, P8	.1" shunt	Digikey	
61	1	XCR5032-10PC44C (NOT 5032C parts)	XYLINX	U5	PZ5032 32 Macrocell CPLD, 5Volt (not 5032C)	XYLINX	XCR5032-10PC44C
62	1	LM78L12ACZ	NATIONAL SEMICONDUCTOR	U7	12V, 0.1A Voltage Regulator	Digikey	LM78L12ACZ-ND
63	1	2-640362-3	AMP	SOCK 3	28 Pin Dip Socket 600 mil	Digikey	A9328-ND
64	1	LM2574M-5.0	NATIONAL SEMICONDUCTOR	U19	Fixed 5.0 V 0.5 A SWITCHING REGULATOR	Digikey	LM2574M-5.0-ND
65	2	LM2574M-3.3	NATIONAL SEMICONDUCTOR	U17, U18	Fixed 3.3 V 0.5 A switching regulator	Digikey	LM2574M-3.3-ND
66	1	M27C512-70XF1	SGS-THOMSON	U9	64K x 8 70 nsec EPROM	Digikey	NM27C512Q90-ND
67	1	P89C51RD+	PHILIPS	U2	80C51 Microprocessor 44 Pin PLCC FLASH PGM	Philips	P89C51RD+

68	1	PDI1394L41/L40	PHILIPS	U12	Philips Link IC	Philips	PDI1394L41/L40
69	5	None	Various	P23,P24,P25,P26,P27	6-32 x 1/4 screw phillips panhead	Digikey	H354-ND
70	1	DPS150100-P5	CUI STACK	P16	15 V Regulated Power Supply 120 VAC Wall mount	Digikey	T924-ND
71	1	SG636PCE-22.118MC2	EPSON	U1	22.118 Mhz 3 - 5V clock oscillator	Digikey	SE2835-ND
72	5	Unknown	KEYSTONE	P18,P19,P20,P21,P22	Hex Spacer, Threaded Nylon, 6-32 thread .750"lng	Digikey	1903DK-ND
73	1	18548	3M	P17	10" x 12" anti static bag	Digikey	SCP170-ND
74	1	AK131-2	ASSMANN	P28	Serial Cable 9 pin male to 9 pin female	Digikey	AE1020-ND
75	1	CFWA-66-3.3	LYNN PRODUCTS	P29	Fire wire Cable, 1 meter long	LYNN PRODUCTS	CFWA-66-3.3
76	1	2774-SPC	SPC TECHNOLOGIES	P30	25 pin female to 9 pin male adapter connector	Newark	92N5316
77	1	HF-0787	MURATA	U15	DC-DC Converter 5V IN, 3.3V OUT	Murata	HF-0787
78	3	4N36	QUALITY TECHNOLOGIES	ISO 1, ISO 2, ISO3	Optocoupler, 4N36, Transistor output	Digikey	4N36QT-ND
79	1	P6.8KE39CAGICT	GENERAL SEMICONDUCTOR	D14	Bi Directional Transient Absorber, 600W, 39V	Digikey	P6KE39CAGICT-ND
80	1	ECJ-2VB2A332K	PANASONIC	C68	3.3 nF 50v 0805 capacitor	Digikey	PCC1988CT-ND
81	2	9.1K RESISTOR, SM	PANASONIC	R16,R104	9.1K Resistor, 0805	Digikey	P9.1KACT-ND
82	2	13K RESISTOR, SM	PANASONIC	R14,R105	13 K Resistor, 0805	Digikey	P13KACT-ND

Appendix B: Evaluation Board Schematics

The following pages are re-printed hardware schematics of the Evaluation Board.



NOTES: UNLESS OTHERWISE SPECIFIED.

1. ALL RESISTORS IN OHMS AND 0805 PACKAGE.
2. ALL POLORIZED CAPS ARE ELECTROLITIC EXCEPT AS NOTED ON THE SCHEMATIC

NEXT ASSEMBLY	USED ON
APPLICATION	

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCE
ANGLES +/- .5 °
FRACTIONS +/- —
DECIMALS .XXX+/- .010 .XX +/- .03
PART SHALL BE FREE OF BURRS
BROKEN EDGE —- MAX
FILLET R —- MAX
SURFACE ROUGHNESS -----
INTERPRET DRAWING IN ACCORDANCE WITH MIL-STD-100 ANSI Y14.5M-1982

CONTRACT:
L4X RDK Board Rev 2 Layout

	DATE
DWN	
CHK	
ENGR	
QA	
APVD	

PHILIPS SEMICONDUCTORS
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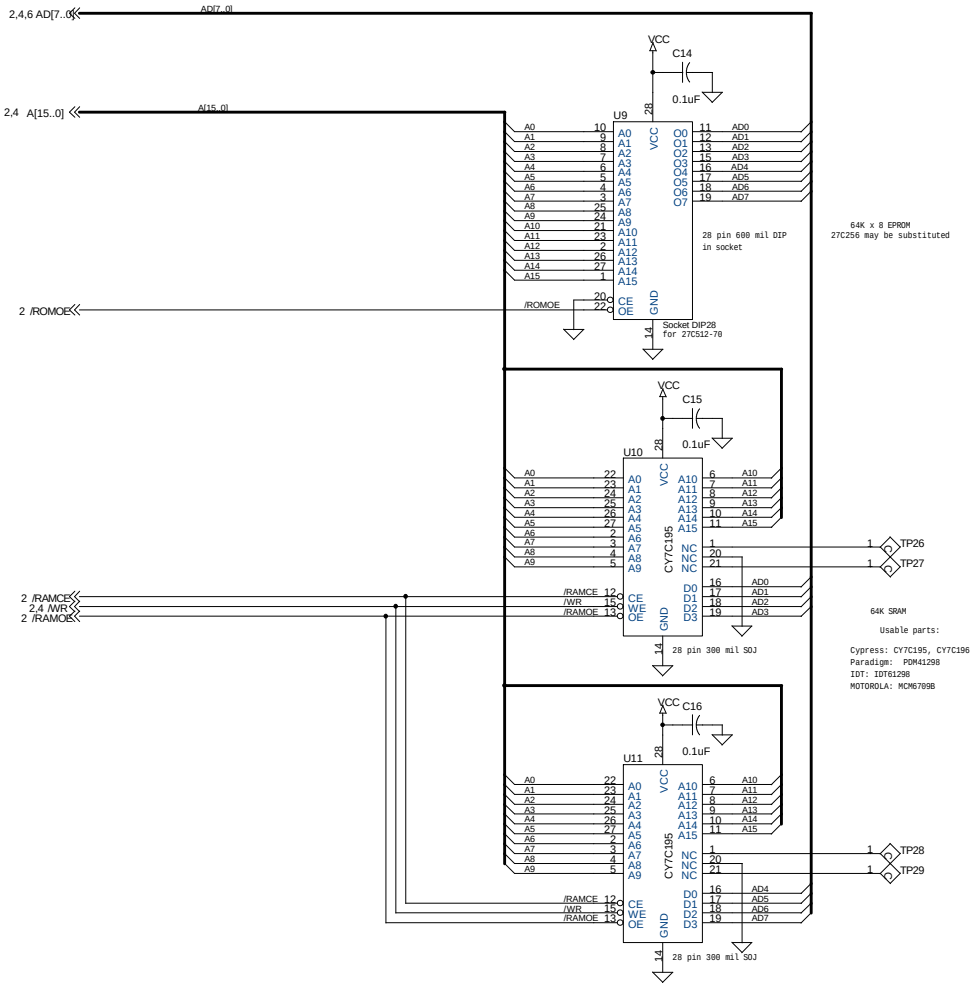
ALBUQUERQUE NE, 87113
1394@PHILIPS.COM

SCHEMATIC DIAGRAM, L4X RDK

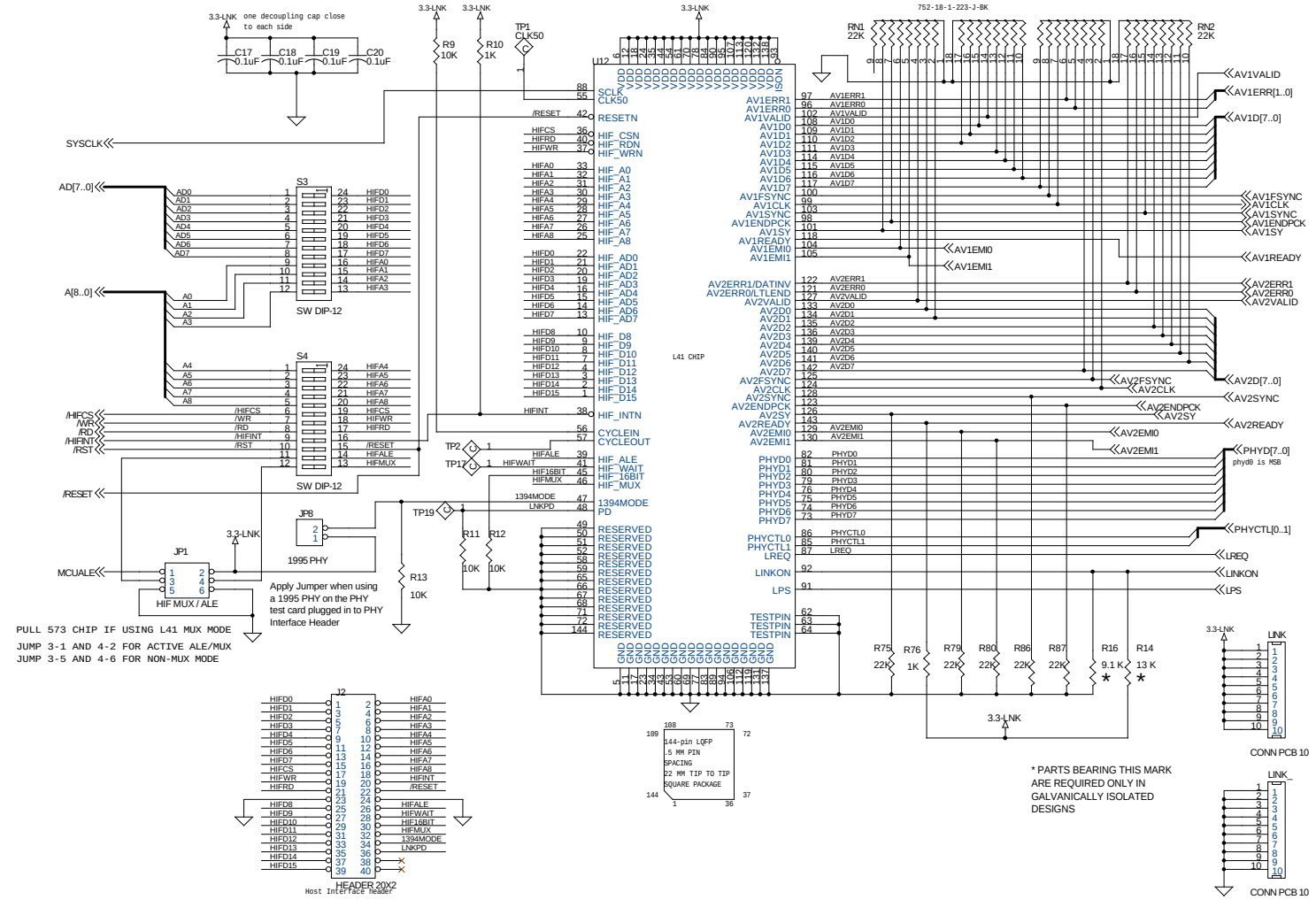
SIZE	CAGE CODE	DWG NO.	REV
D		PH000801-103	0
SCALE NONE			SHEET 1 OF 8

1394 Micro. Interface - Memory



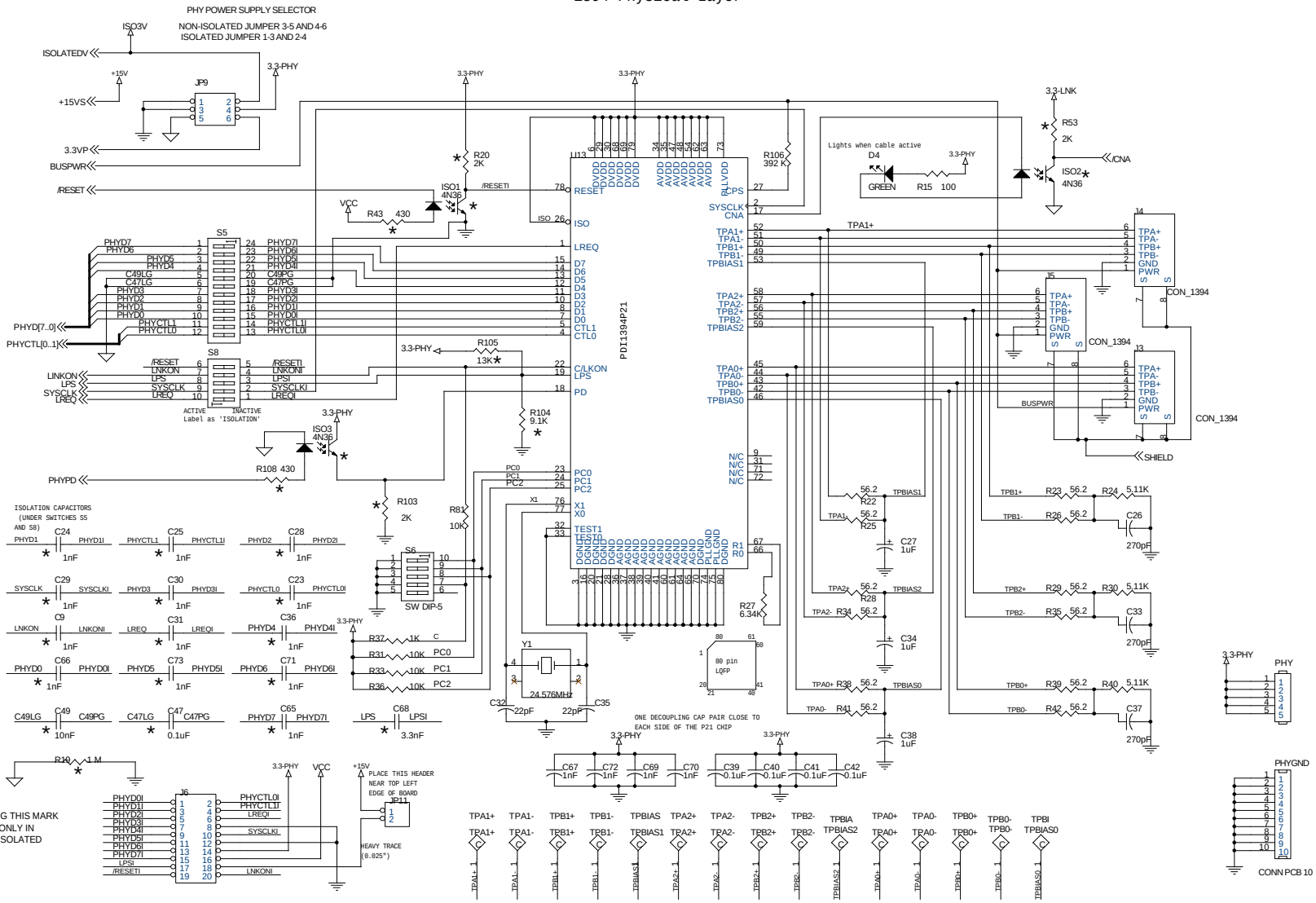
PHILIPS SEMICONDUTORS ALBUQUERQUE NM, 87113	CONTRACT: L4X RDK Board Rev 2 Layout			
	SIZE	CAGE CODE	DWG NO.	REV
	D		PH000801-103	0
DWN				
	SCALE NONE			SHEET 2 OF 8

1394 Link Layer



PHILIPS SEMICONDUTORS ALBUQUERQUE NM, 87113	CONTRACT: L4X RDK Board Rev 2 Layout		
	SIZE D	CAGE CODE	DWG NO. PH000801-103 REV 0
DWN	SCALE NONE		SHEET 3 OF 8

1394 Physical Layer



PHILIPS SEMICONDUTORS ALBUQUERQUE NM, 87113	CONTRACT: L4X RDK Board Rev 2 Layout		
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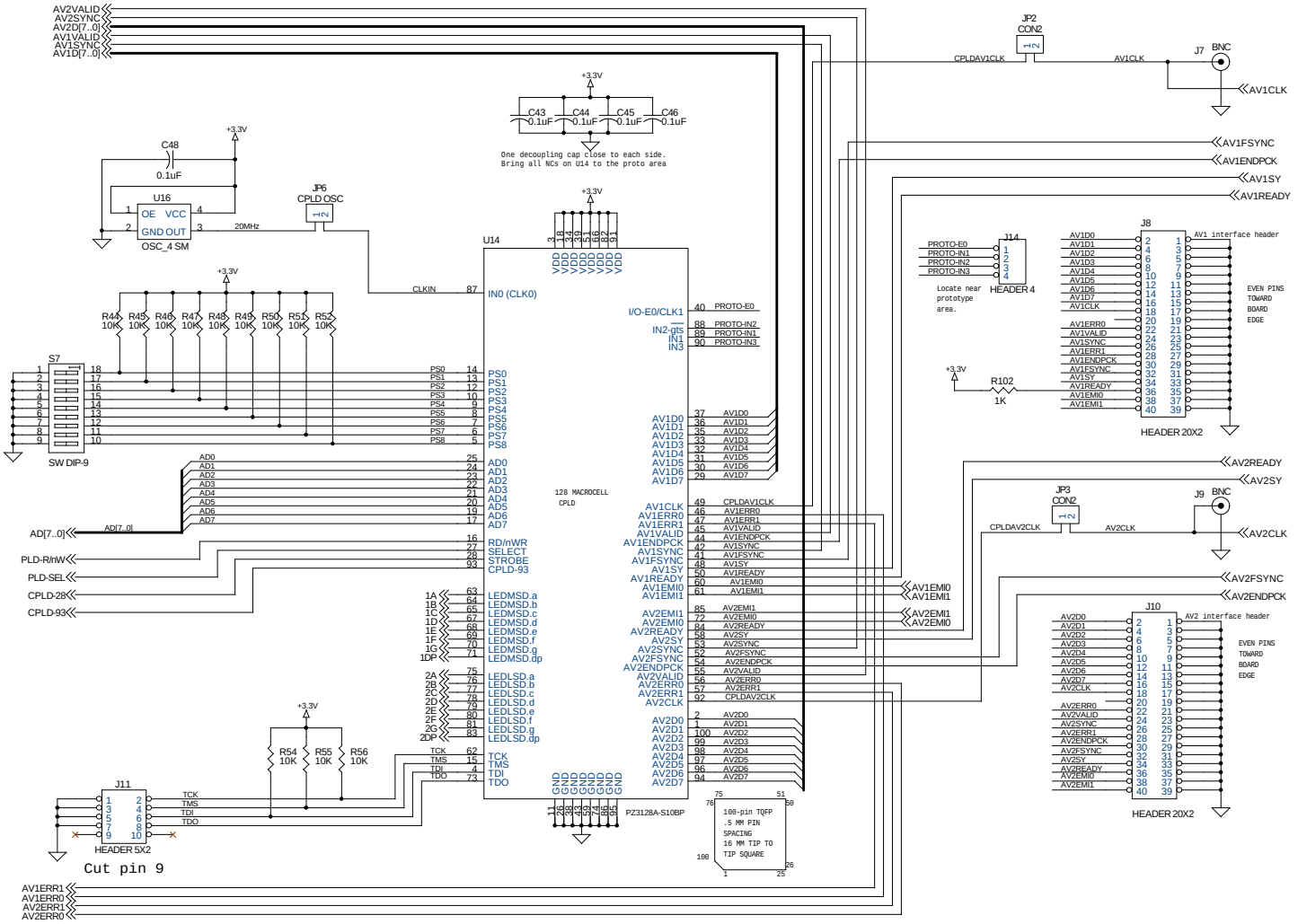
			REV: 0
DWN	SCALE: NONE		SHEET: 4 OF 8

1394 AV Interface



PHILIPS SEMICONDUTORS ALBUQUERQUE NM, 87113	CONTRACT: L4X RDK Board Rev 2 Layout			
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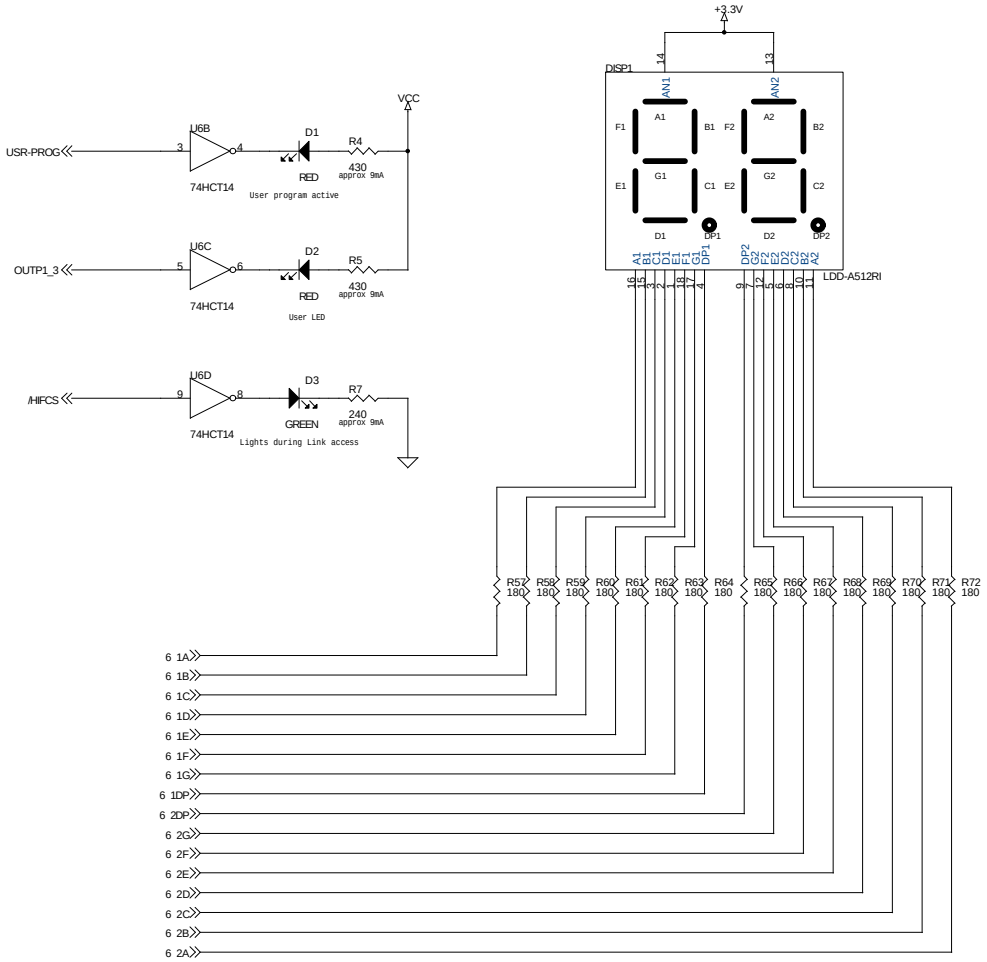
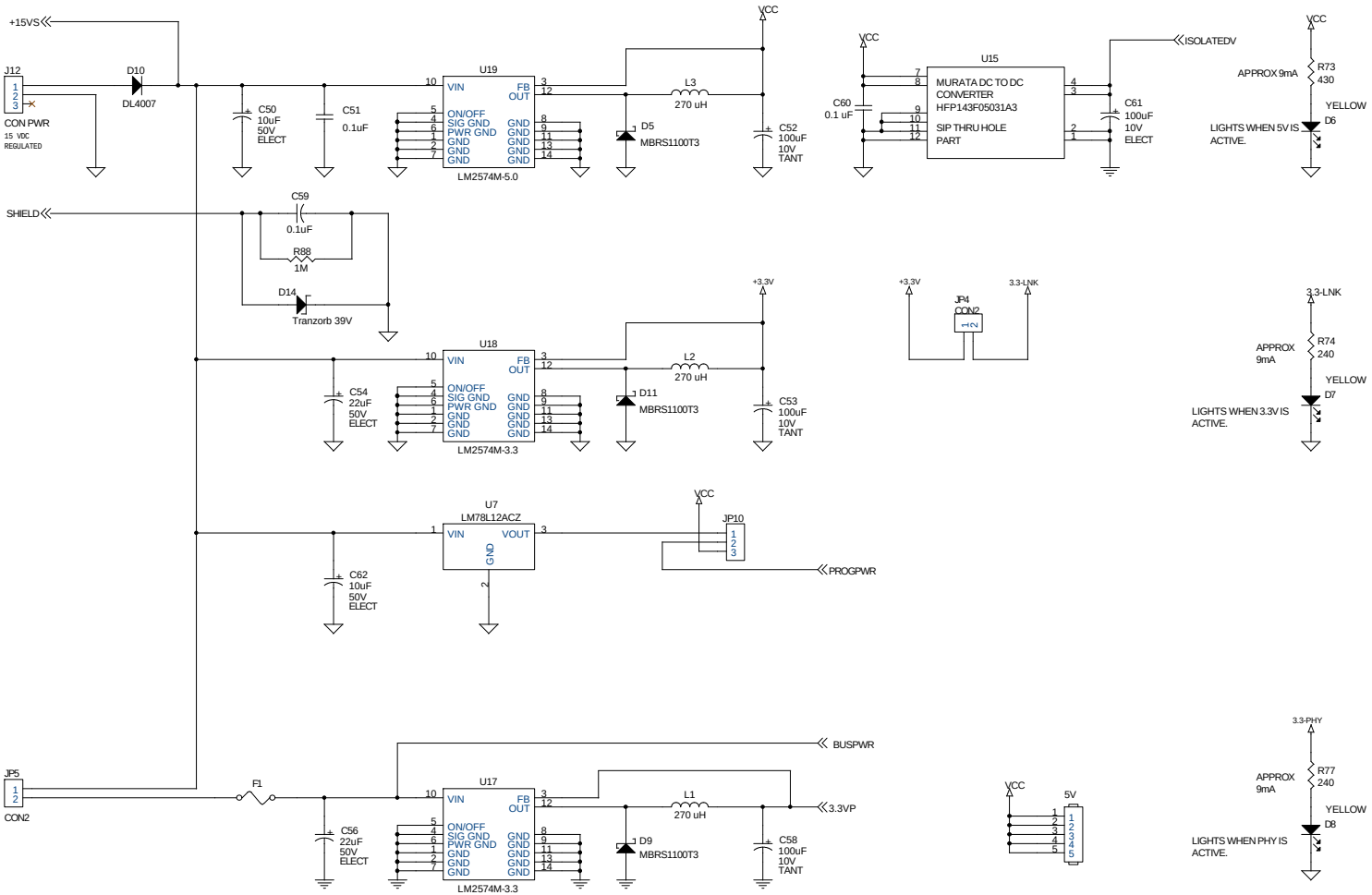
DWN	SCALE NONE			SHEET 5 OF 8



PHILIPS SEMICONDUTORS ALBUQUERQUE NM, 87113	CONTRACT: L4X RDK Board Rev 2 Layout			
	SIZE D	CAGE CODE	DWG NO. PH000801-103	REV 0
DWN				
	SCALE NONE		SHEET 6 OF 8	

1394 POWER



PHILIPS SEMICONDUTORS ALBUQUERQUE NM, 87113	CONTRACT: L4X RDK Board Rev 2 Layout			
	SIZE	CAGE CODE	DWG NO.	REV
	D		PH000801-103	0
DWN				
	SCALE NONE		SHEET	7 OF 8

1394 Passive Parts

P1 SHUNT
P2 SHUNT
P3 SHUNT
P4 SHUNT
P5 SHUNT
P6 SHUNT
P7 SHUNT

P8 STAPLE
P9 STAPLE
P10 STAPLE
P11 STAPLE

Parts that go in sockets

MCU
SOCK 1
P89C51RD+
for U2

SOCK 2
PZ5032
for U5

EPROM
SOCK 3
27C512-70
for U9

SOCK 4
PDI1394L4X
for U12
proto production (10 units)

PCB
P15
PCB

Power Supply
P16
15V PS

Spacers (legs)
P18 spacer
P19 spacer
P20 spacer
P21 spacer
P22 spacer

P23 screw 6-32
P24 screw 6-32
P25 screw 6-32
P26 screw 6-32
P27 screw 6-32

anti-static bag
P17
as bag

Serial cable
P28
serial cab

Firewire cable
P29
1394 cab

25 pin to 9 pin converter
P30
25to9

PHILIPS SEMICONDUTORS ALBUQUERQUE NM, 87113	CONTRACT: L4X RDK Board Rev 2 Layout			
	SIZE	CAGE CODE	DWG NO.	REV
	D		PH000801-103	0
DWN				
	SCALE NONE		SHEET 8 OF 8	